Microwave Interaction of Thermal Electrons in Semiconductors

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MICROMINIATURIZATION OF INTERNAL ELECTRONICS "MICROELECTRONICS" (U)

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FOR THE COMMANDER
Approved By

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Chief, Laboratory 50

FOREWORD

The text of this report was given as a paper at the Second National Convention on Military Electronics, sponsored by the PGME, IRE, at Washington, D. C., on June 16 - 17 - 18, 1958.

MICROMINIATURIZATION OF INTERNAL ELECTRONICS - "MICROELECTRONICS"

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Abstract

This paper is a progress report on one approach to the problem of fabricating small electronic circuits. Printed circuit and metal evaporation techniques have been used to produce a binary counter module occupying less than 1 1/0 of a cubic inch. Included in the module are two transistors, two diodes, two capacitors, and eight resistors. Problems and solutions are described in the areas of circuit design, passive component, semiconductor component, and encapsulation. Extrapolation of present techniques shows promise of permitting a density of 2000 transistors plus associated components per cubic inch.

Introduction

Modern weapons are placing increased demands on ordnance electronics. One severe requirement is the need to put more electronics in less space. The Diamond Ordnance Fuze Laboratories have been active for more than a decade in the areas of printed circuitry and subminiaturization. Approximately a year ago a team of circuit, component, and semiconductor people was formed to concentrate on the problem of making radically small electronics. This present paper is a progress report on the year of activity in microminiaturization at DOFL.

Two stages in the evolution of the methods of making small electronic packages will be described. The first step will be covered briefly as it is a logical extension of the etched wiring board incorporating separately cased component parts such as the Signal Corps Auto-Sembly[1] technique. The second step is the utilization of printed circuit techniques wherever possible.

The term "internal electronics" is used to describe that portion of an electronic system that operates at low power level and is primarily concerned with the handling and processing of information. Not included are the usual high power stages required to drive motors, antennae or display devices. These latter circuits occur at the boundary between the electronic system and the environment surrounding it.

"Hearing Aid" Approach

The advent of small resistors, capacitors, and transistors as used by the hearing aid industry has permitted etched wiring boards to be scaled down in size. The amount of reduction is roughly in proportion to the reduction in size occurring between commercially available 1 watt resistors and 1/10th watt resistors. This approach has brought up new problems in fine line etching, component insertion and dip soldering because of the closer physical tolerances demanded. However, the progress in etched board technology has made the step less difficult.

Figure 1 shows several modules made by this approach. About 150 component parts, 20 transistors plus associated parts, or 10 binary counter stages per cubic inch is the possible density. Interconnection of the individual modules is accomplished by means of a secondary etched board.

Method of Quantitative Comparison

A brief digression is in order to discuss how to compare the various fabrication schemes in a quantitative manner. Three densities will be used:

(1) Total number of component parts per cubic inch.
(2) Number of transistors per cubic inch. Other component parts are assumed fitted in also.
(3) Number of binary counter stages per cubic inch.

The component man generally likes the first density. The circuit man likes the second because it is an indication of the number of active elements. The logic designer favors the third because it is a measure of the logical blocks that can be fit into a cubic inch.

DOFL 2D Approach

As pointed out by Brunetti[2] the significant reduction in size comes about by eliminating individual part cases and blending the parts into one heterogeneous mass. The integrated-caseless printed circuit approach under study at DOFL is a start in this direction.

Some general guidelines were used to direct the search for techniques. As mentioned above no individual component protection was to be used unless absolutely necessary. Secondly, rather than attempting to reduce all three dimensions an equal amount it was decided to concentrate on a "two dimensional" module with the third dimension, i.e., the thickness, as thin as possible. This permits approaching zero volume but with a finite area that can

[1] S.G. Bassler, "The Application of Auto-Sembly to the Missile Field," Convention Record of First National Convention on Military Electronics, 1957, pp. 109-116

[2] C. Brunetti, "A New Venture into Microminiaturization," 1957 IRE Convention Record, pt. 6, pp. 3-10.

still be seen and worked on. The third point was to demand the least in performance out of the individual component parts. This latter point was particularly important when considering the possibility of using caseless transistors.

Problem Areas

A number of interrelated areas of work were involved in the successful design and fabrication of working modules. Included were:

1. Choice of circuit type and constants.
2. Mounting plate, conductors, resistors, and capacitors.
3. Semiconductor components (diodes and transistors).

Additional areas being worked on now are:

4. Transistor-diode protection from contamination.
5. Over-all protection of a module.
6. Interconnection of modules.
7. Optimum complexity of modules.
8. Environmental evaluation.

The circuit chosen for experimentation in working out the techniques was a binary counter stage. This type circuit can be designed to operate with broad margins and thus permit early fabrication of working circuits for study under dynamic conditions. The circuit schematic is shown in Figure 2. No attempt was made to obtain high frequency performance. The capacitors are large enough in capacity for use with low-frequency audio-type transistors.

The counter circuit is tolerant in demands on the component parts in several respects:

1. low frequency (as mentioned above),
2. low voltage operation,
3. low current operation,
4. low transistor current gain (β) permitted,
5. high transistor I_{CBO} permitted,
6. resistor ratios more important than absolute values.

In the fabrication of modules much of the technology developed in the past ten years for printed circuits has been directly applicable with proper scaling down in size. The mounting plate used in the modules is a steatite ceramic wafer 1/2 inch square by 20 mils thick. The conductor pattern is a silk screened silver paint fired in place. The conductor width is approximately 50 mils.

The resistors are also silk screened on the wafer and are a carbon composition similar in characteristics to commercially available composition resistors. A 10K ohm resistor is approximately 60 mils square and 1 mil thick.

Injection molding methods look attractive for large production runs.

The capacitors used are an experimental type made from reduced barium titanate. The 0.01 μf capacitor is physically 0.1 inch square and 8 mils thick. This type capacitor has a very low voltage breakdown, a property which does not prevent its use in the present modules.

The most difficult problems occur in obtaining a satisfactory caseless transistor. Mounting the die, lead attachment, and surface protection constitute the major difficulties. The particular transistor type utilized in the first operating modules is a diffused-base unit. The 45 mil square die is cemented in a hole in the ceramic plate with epoxy plastic. Connections are made between the transistor electrodes and the silver wiring pattern by an evaporated aluminum film. The precise dimensional control required is obtained by photolithographic techniques.[5]

An experimental module is shown in Figure 3. The back side is identical in construction. The silver wiring pattern, black resistor pattern, capacitor plates, and semiconductor devices are clearly visible. This 2D approach will permit a density of about 1500 component parts, 200 transistors plus associated parts, or 100 binary counter stages per cubic inch.

The protection of the individual component parts and the completed modules is being approached from several aspects. The semiconductor devices are undoubtedly the most vulnerable. The photoresist used to make the diffused base type transistors has proven to be a good surface protector. Other plastic encapsulants are being considered for temporary protection purposes. The present plan is to hermetically seal a number of interconnected modules into a common container. Poisoning of the semiconductor surfaces by contaminants from the other component parts in the same sealed volume is being investigated. If necessary it may be possible to individually seal each transistor or diode in its hole in the ceramic plate.

The interconnection of power and signal lines between modules must be done in an efficient and practical fashion or the large volume reduction theoretically obtainable will not be achieved. One face of a group of stacked

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[5] J. R. Hall and J. W. Lathrop, "Photolithographic Fabrication Techniques for Transistors which are an Integral Part of a Printed Circuit," A paper presented at the 1957 Electron Devices Meeting of the IRE PGED, Nov. 1, 1957.

modules can be used for interconnections. The binary counter module has lead wires coming out one end. A small etched interconnection board can be used in a similar fashion to the "hearing aid" approach.

An experimental technique being tried is to chemically deposit copper or screen silver as the interconnection pattern directly on one or more faces of the group of modules.

A particularly troublesome question which must be [illegible]ved in a specific system application is: what [illegible]er of components or degree of complexity should module have? Making the modules too [illegible]e will mean a large and complicated interconnection pattern. If the modules are [illegible]y complicated the yield in production will be low and the cost to replace a defective module will be high. In the present research stage the binary counter is sufficiently involved to tax the techniques under study.

Detailed environmental studies are needed to check the life and ruggedness of the integrated-caseless modules. Temperature extremes, high humidity, shock, and vibration will undoubtedly expose weaknesses in the techniques.

Future possibilities

Although problems still exist in the fabrication of the present size modules even smaller versions seem feasible. Two broad approaches are possible. The most direct is to scale down further the printed components and caseless semiconductor devices. A factor of two decrease in each dimension seems practical and would give another order of magnitude reduction in volume.

A second approach which has greater potential is to integrate the functions of resistors, capacitors, diodes, and transistors, to a much greater extent. In the present approach the various component part types are made in separate distinct steps. If all component parts could be fabricated from one type of material by a single process, such as printing or evaporation, a much smaller and simpler module would result.

In the area of reliability a particularly difficult problem is to assure solid ohmic interconnections between modules. As sizes go down the difficulties rise rapidly. One promising approach is to use only capacitative or inductive coupling between modules.[4] The most important consideration will then become the proper geometric relationship of the modules rather than good low resistance connections. Power and signal connections would all be handled in the same manner. It should be possible to reduce drastically the number of faulty and erratic connections.

Conclusions

Figure 4 summarizes the evolution of fabrication techniques as illustrated by a 10 stage binary counter. The top view shows etched boards with standard component parts. The middle view is the "hearing aid" approach. The small unit at the bottom shows the DOFL 2D technique.

The techniques described permit one to two orders of magnitude reduction in volume of electronic equipment used for information handling purposes. Further research along logical extensions of the present methods show promise of permitting several thousand transistors plus associated components to occupy less than one cubic inch.

It requires little imagination to see many potential benefits of this compact electronics - microelectronics - to the various phases of military electronics. More electronics will be able to go into a given volume or even more important, electronic systems never before considered portable will be easily carried in missiles, satellites, or by man.

Acknowledgements

The work described in this progress report is the result of the efforts of many people. Included are Edith Davies, N. J. Doctor, Dr. J. W. Lathrop, J. R. Nall, A. A. Benderly, and Meyer Schwarz.

[4] This idea is an extension of one proposed by W. D. Fuller and J. G. Smith of Varo Mfg. Company in which only the signal connections would be made by capacitative coupling.

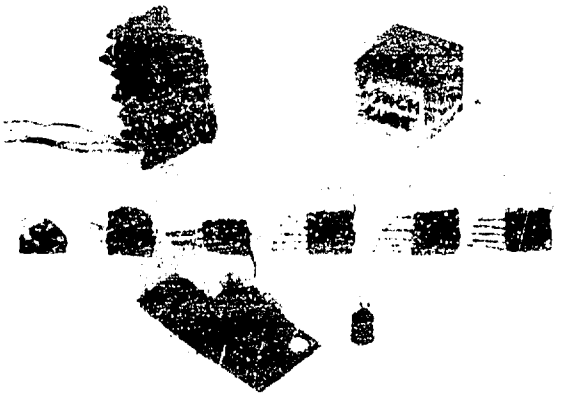

Figure 1. "Hearing Aid" Approach

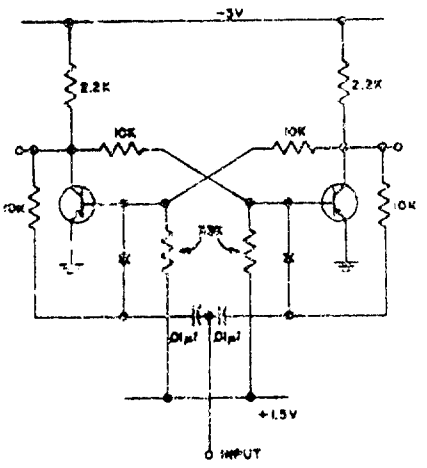

Figure 2. Binary Counter Schematic

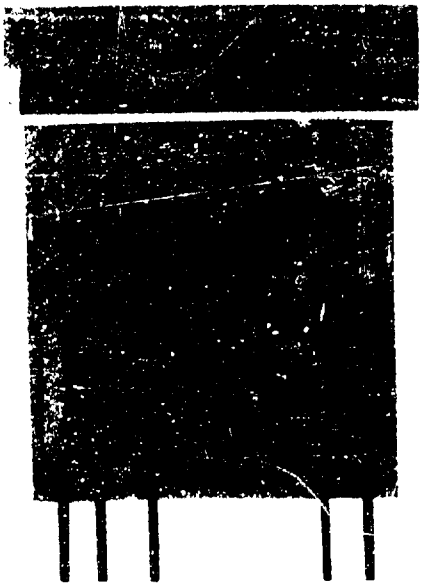

Figure 3. DOFL 2D Approach

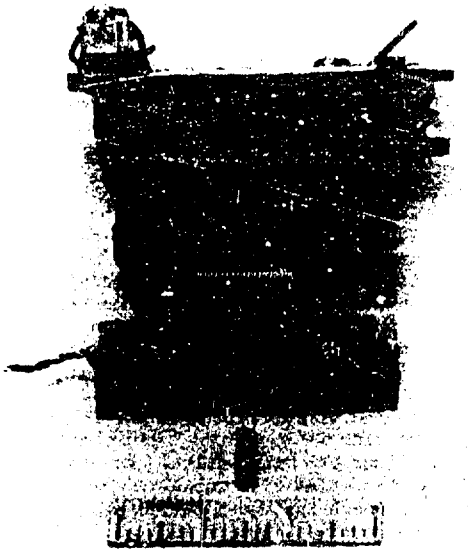

Figure 4. Evolution of Fabrication Techniques

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